



A SystemVerilog Primer

By J. Bhasker

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- Written for new users. - Explains the language through simple examples. - Explains the syntax of language using commonly-used design terminology. - Based on IEEE 1800-2009 - Writing is made easier by providing a number of examples - Many hardware modeling examples also been provided to make this an excellent reference

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Review

" It is an awesome book - on the same lines as your other texts. It is a very good companion to the Verilog Primer and brings out the most important concepts of the SV language with easy to understand examples. " - Preetham Lakshmikanthan, Intel --Email

" A SystemVerilog Primer is an excellent resource to get up to speed on the application of the various features of SystemVerilog per IEEE 1800-2009. The explanations of each feature is provided with examples and guidelines, where appropriate." - Ben Cohen, Author/Consultant --Email

" The book is very useful for someone who just wants to know what the practical elements of the language are and as a quick reference book." - Ambar Sarkar, Paradigm Works --Email

About the Author

Bhasker is an Architect at eSilicon Corporation. He was a Distinguished Member of Technical Staff at Bell Laboratories. He has received a Meritorious Service Award from IEEE Computer Society for his technical contributions and continued leadership in the development of the EDA standards, especially the VHDL and Verilog RTL synthesis standards.

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